Claims

1. A non-volatile memory cell comprising:

a semiconductor substrate, with a drain and a source in said substrate;

a floating gate formed on said substrate, said floating gate including a main floating gate region and a small sidewall spacer electrically coupled together;

a first insulating layer separating said floating gate from said substrate, said first insulating layer including a first insulating portion and a second insulating portion, said first insulating portion separating said small sidewall spacer from said substrate, said second insulating portion separating said main floating gate region from said substrate, wherein, said first insulating portion is thinner than said second insulating portion;

a control gate formed over said floating gate; and

a second insulating layer separating said control gate and said floating gate.

2. The non-volatile memory cell of claim 1 wherein said floating gate further comprises a connecting layer for electrically connecting said small sidewall spacer and said main floating gate region, said connecting layer being formed over and in contact with both said small sidewall spacer and said main floating gate region.

3. The non-volatile memory cell of claim 2 wherein said small sidewall spacer resides along a side and on top of said main floating gate region.

4. The non-volatile memory cell of claim 3 wherein said first insulating portion is over said drain.

5. The non-volatile memory cell of claim 4 wherein said drain and source are self-aligned with the opposing sides of said main floating gate region.

6. The non-volatile memory cell of claim 1 wherein said small sidewall spacer resides along a side and on top of said main floating gate region.

7. The non-volatile memory cell of claim 1 wherein said first insulating portion is over said drain.

8. The non-volatile memory cell of claim 1 wherein said drain and source are self-aligned with the opposing sides of said main floating gate region.